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Effects of scaling on the characteristics of CMOS analog circuits

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Ефекти на мащабирането върху характеристиките на аналогови CMOS схеми

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Abstract: *Continued scaling of CMOS technology affects both, the parameters and the characteristics of MOSFET and the integrated circuit built on them and introduces some new problems in analog design. The reduction of the gate length and the gate oxide thickness led to improvements in terms of chip area, speed and power consumption. At the same time, nonlinear output conductance, reduced voltage gain and gate-leakage currents, set limits to analog circuits performance. In this paper are analyzed some characteristics of MOSFET (currents, I-V characteristics), considering different technology nodes. The impact of scaling below 0.1 μm on the characteristics of the analog circuit is evaluated by the device simulation of an operational transconductance amplifier (OTA) using LTspice simulation tool.*

Key words: *CMOS, integrated circuits, simulations, scaling*

INTRODUCTION

Advance in wireless and wireline communications and emerging new applications, such as ultra-wideband and 60-GHz-band systems or next-generation cable modems, has increased the interest for analog applications of MOSFETs, and has become the driver for developing high-resolution, high-speed, low power, and low cost integrated analog to-digital converters (ADCs) [1,2].

Technology scaling increased the density of the digital circuits while reducing the circuit delays and cost. For the analog circuits, the reduction of the channel length (L), gate oxide thickness (t_{ox}) and the power supply voltage resulted in the increased device speed and lower power consumption for each new node. However, 90 nm technology generation and next (65 nm, 45 nm) brought new challenges to integrated circuit (IC) designers [3] According to the International Technology Roadmap for Semiconductors (ITRS) [4], some fundamental limitations to MOSFET scaling are quantum mechanical tunneling, the randomness of discrete doping, and the increasing power dissipation.

Studies on the impact of scaling on the analog devices performance are important due to the increased interest in CMOS analog applications. In [5] the influence of scaling on the performance of small-signal MOS amplifiers is evaluated by analytical models and physics-based device simulation. The limitations set by non-ideal scaling of the electrical characteristics of the MOSFET and their influence on the trade-off between power dissipation and performance were analyzed.

Muñiz-Montero et al. proposed a differential flipped voltage follower class-AB with improved power management under dynamic conditions, and the enlarged signal swing and dynamic range [6].

The Simplex particle swarm optimization technique was used in [7] for analog ICs optimization (a CMOS two-stage comparator and a folded cascade operational transconductance amplifier), towards the aim to adjust the design variables (device dimensions) and dc bias currents.

The aim of our work is to investigate how the technology notes alter the parameters of MOSFET (drive and leakage currents) and to investigate the effects of device scaling below 100 nm on the gain and the bandwidth of a CMOS operational transconductance amplifier (OTA), which is a basic building block of more complicated analog circuits. The simulation results of the OTA for 50 nm technology are presented.

RESULTS

The evaluation of the impact of the technology generation on some relevant MOSFET parameters was done by means of TAMTAMS Web tool [8]. This is an open tool for process-to system analysis, which allows estimating the scaling effects on both, device and system performance [9]. Device level analysis show the scaling behavior of most important electrical parameters of MOSFETs, such as: drive current I_{on}, leakage currents I_{off}, I_{gate}, threshold voltage V_T, electrons/holes mobility, ratio between the supply voltage and the threshold voltage V_{DD}/V_T etc. Parametric analysis can be done using different kind of parameters, e.g. ambient parameter (temperature) or processing parameter (gate oxide thickness).

Fig. 1 shows I_{on} scaling behaviour of an *n*-channel and a *p*-channel MOS transistor for several technology nodes.

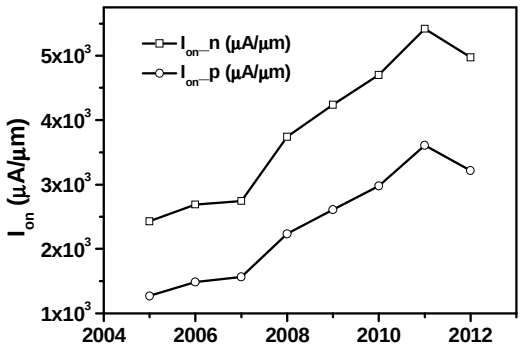

Fig.1. I_{on} versus technology node.

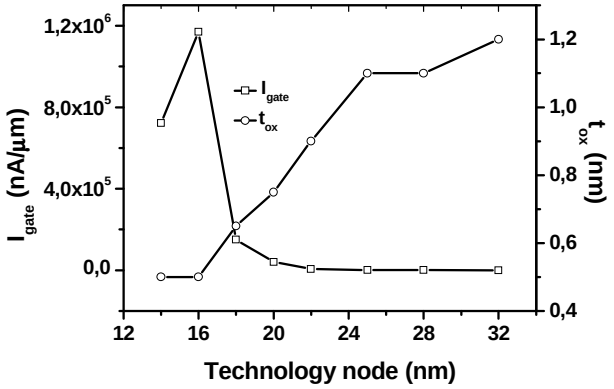

Fig.2. The relationship between the gate leakage current, gate oxide thickness and the technology node.

The reduction of channel length from 32 nm 14 nm resulted in the increase of the I_{on} current by a factor of two from 2430 µA/µm to 4974.6 µA/µm.

Tunneling current through the gate oxide is one of the main limitation factors to scaling. In Fig. 2 is plotted the relationship between the gate current, gate oxide thickness and the technology note. According to simulation results, 1.2 nm thick SiO_2 (2005) will have a leakage current of about 0.005 A/cm at 1.1 V, while for 0.5 nm thick SiO_2 (2012) it will be 7 A/cm at 0.9 V.

Circuit simulations were performed on operational transconductance amplifier (Fig.3) using LTspice симулатор. Short channel 50 nm BSIM4 MOSFET model (V_{DD}=1V), level = 54 was used. The characteristics of OTA with MOSFET's channel length of L =100 nm were compared with the characteristics of OTA with two times reduced MOSFET's channel length of L =50 nm).

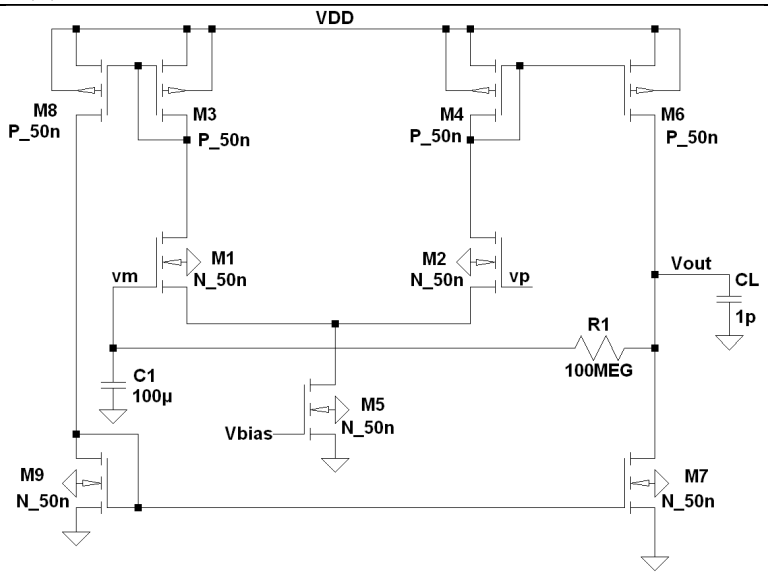

Fig.3. Schematic of simulated OTA.

The drain current per channel width for the MOSFET biased in saturation region is altered by CMOS technology evolution

$$\frac{I_D}{W} = \frac{\mu_n \varepsilon_0 \varepsilon_{ox}}{2(kt_{ox})(kL)}(kV_{GS} - V_T)^2 \qquad (1)$$

where k is the scaling parameter, μ_n is the electron mobility, ε_0 is the vacuum permittivity, ε_{ox} is the relative dielectric constant of the oxide, L and W a channel length and width respectively.

In Fig. 4 are compared simulated *I-V* characteristics of two *n*-channel MOSFETs with the channel lengths of 50 nm (M1) and 100 nm (M2).

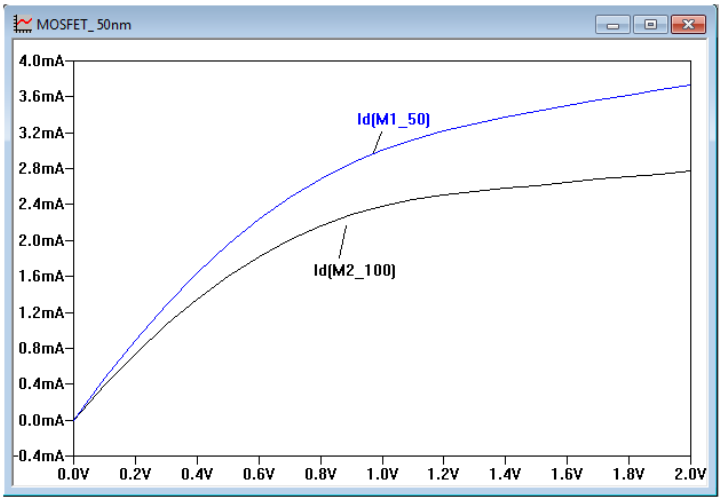

Fig.4. I-V characteristics for two MOSFETs: M1 - 50 nm (length), 2.5 µm (width); M2 - 100 nm (length), 5 µm (width).

The voltage gain of OTA is given by [10]

$$A_V = \frac{v_{out}}{(v_p - v_m)} = kg_m(r_{o6} \| r_{o7}) \qquad (2)$$

where g_m is the transconductance and r_{o6} and r_{o7} are the output resistances of M6 and M7.

Fig.5 shows the AC analysis of OTA. The simulation results show that two times reduction of *L* and *W* causes degradation of the voltage gain e.g., as *L* is scaled from 100 nm down to 50 nm, the voltage gain is scaled down by a factor of 0.6, from 28 dB to 16.8 dB. According to [5] the degradation is mainly due to: (i) mobility degradation at large doping levels and non-ideal scaling of gate capacitance; (ii) short-channel effects.

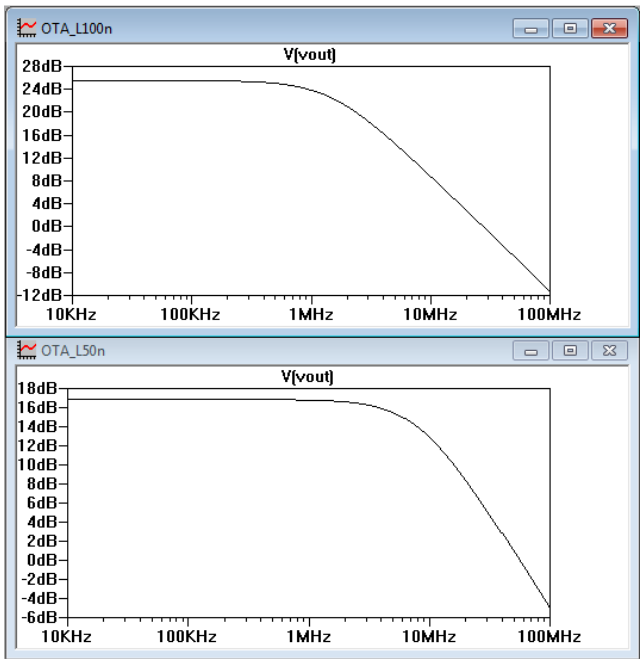

Fig. 5. AC analysis of the OTA with L=100nm and L=50nm.

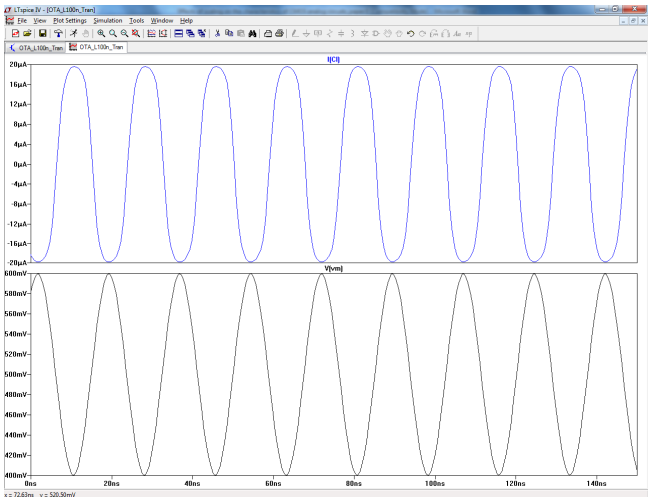

Fig.6. Transient analysis of the OTA (L=100nm).

The amplifier's bandwidth is limited by intrinsic capacitances. The unity gain frequency was found to be 27 MHz and 57 MHz approximately for 100 nm and 50nm respectively. This result is in good agreement with other authors observations [11].

The output current of OTA is given by

$$I_{out} = g_m (V_p - V_m) \qquad (3)$$

The transient analysis of OTA (Fig.6) shows that the output current of the schematic with reduced channel length and width is higher than the output current of OTA with *L* =100 nm MOSFETs.

CONCLUSIONS

The evaluation of the impact of the technology node on some relevant MOSFET parameters was done. Circuit simulations are performed to investigate the effects of scaling on the characteristics of operational transconductance amplifier for 50 nm technology using a short channel BSIM4 model (V_{DD}=1 V).

The reduction of channel length from 32 nm 14 nm resulted in the increase of the I_{on} current by a factor of two from 2430 μA/μm to 4974.6 μA/μm. The gate leakage current increases exponentially with decreasing t_{ox} from 0.005 A/cm (t_{ox} = 1.2 nm) to 7 A/cm (t_{ox} = 0.5 nm).

The simulation results show the reduction of the voltage gain from 28 dB to 16.8 dB and the increase of the unity gain frequency and the output current as *L* is scaled from 100 nm down to 50 nm.

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