A comprehensive workflow and methodology for parasitic extraction

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Abstract: *In this paper is presented, analysed and assessed a design automation methodology of a tool employed for parasitic extraction. A brief background of the parasitic extraction process and the tool operation is initially outlined. The paper then focuses on the automation flow, deeply examining input and output files. An explanation of the methodology is included, in conjunction with a Techgen cell flow and commands. It is concluded by analysing an extract of the results.*

Key words: *Parasitic extraction, digital design automation, transistor level design, cell level design, digital design flow, top layout, top netlist, techgen cell flow, QRC*

INTRODUCTION

The contemporary integrated circuit creation process has ever-increasing steps and complexity. This trend has been in existence since decades and carries on. For instance, the creation methodology is consisted of four separate major phases: design, synthesis, place and route and signoff. Each of them is made up of distinct steps – for signoff they are: design check, rail analysis, static timing analysis, dynamic simulation, formal equivalence check, power analysis, simulation and verification, as each of them is devised from sub steps and so forth. In other words, the whole process could be described as an hierarchy in which each step is a paragraph, consisted of its own sub steps, represented as sentences, whose sub steps are words and so forth, up to the foundation bottom, where are letters and sounds [2].

The parasitic extraction is a part of the IC creation process, hence could readily be found as a member of the design check at the signoff phase, encountering absolutely the same challenges as the IC methodology itself. More specifically, shrinking semiconductor process dimensions and permanently increasing clock speeds on one hand, mingled with growing number and density of metal layers at each new process node on other hand, are introducing myriads of new parasitic effects in designs. That is why, this step assumes an increasingly important role and is vital for the production of prosperous silicon chips. Furthermore, another confirmation of this statement could easily be found in the fact, that there is wide variety of automated tools coming with the task to ease the fulfilment of the manipulation. Some of them are: Cadence QRC, Synopsys StarRC, Mentor graphics Calibre xRC, Magma QuickCap, Zeni Eda PE, Tanner Eda HiPer PX and Silvaco extractors [3].

Nevertheless, in a stark contrast to the tremendous tool availability, it cannot be claimed the same about the documentation. Moreover, despite the tool constantly carries on increasing importance, there is not a wide diversity of comprehensive workflow together with methodology and commands description readily available. This paper endeavors to bridge the gap by proposing, describing and analysing a possible solution based on Cadence QRC extraction tool.

PARASITIC EXTRACTION TOOL

The parasitic extraction tool deals with the limited ideality of the wiring in an IC, also known as backend. Wires have limited conductivity and are capacitively coupled between each other and to the underlying substrate. The extraction process lumps these effects into additional parasitic devices (capacitors, resistors and inductors), which could be merged with the original netlist. In other words, all parasitics are not initially designed, but are in existence and therefore must be taken into consideration.

Due to the fact that, the cell delay is a function of capacitive parasitics only, it could

be conferred that they have the greatest importance and usually directly affect the whole functionality of the chip. The dependability is directly proportional: the larger are capacitive parasitics the larger is the cell delay.

The parasitic tool commonly requires special foundry data – deck that needs to be provided and quality assured by the technology manufacturer. It is most frequently into a process design kid (PDK) form, containing process models and technology data.

In this article Cadence tool, called QRC is presented. It has been picked thanks to the following advantages:

- Fully integrated as a part of the Cadence design flow environment;
- Supports process variations and PDK-foundry data;
- Ease of use and dependability.

During parasitic extraction, QRC analyses each conductor layer, generates parameters and passes them to the technology file models for capacitance calculation [4].

There are two kinds of parasitic extraction – coupled and decoupled. Although, the first one takes into account the mutual capacitance between nets (nodes), whereas the second – between nets and either previously specified ground net or substrate ground (see Figure 1), both types always require a definition of the ground net. In the paper is calculated decoupled capacitance extraction because coupled has a minor impact over 90/130nm, where wire aspect ratios (w/h) are large and area capacitances dominate [3].

In Figure 1 the decoupling factor represents a derating factor to the extracted decoupled capacitance, offering the ability to change the results from conservative to liberal.

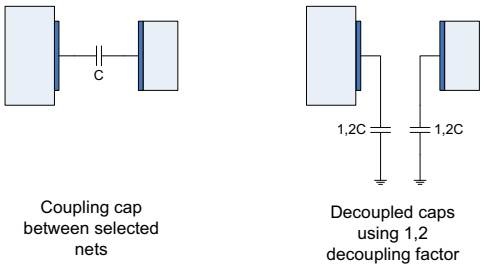

Figure 1 Coupled and decoupled parasitic extraction

On Figure 2 is illustrated the so cold floating node example, containing both coupled and decoupled capacitance. M1 is a floating node on metal1 with capacitive coupling to ground (C1,0) and to M2 (C2,1), M2 is a metal layer with capacitance to ground (C2,0). With the removal of M1, the capacitors C1,0 and C2,1 are merged serially. However, that leaves two parallel capacitors between M2 and ground (C2,0 and the merged C1,0/C2,1 cap). These two capacitors can be merged in parallel to further reduce the parasitic capacitor count of the design.

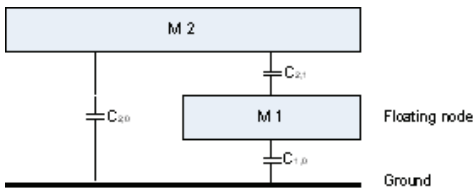

Figure 2 Floating node

AUTOMATION WORKFLOW

There are two different workflows for parasitic extraction: transistor and cell level. During cell level extraction parastics are extracted down to cells, including routing layers, whereas during transistor level – down to components and devices. At large, the cell level extraction is applicable to the digital workflow, whereas the transistor level – to the analogue.

In a contrast to the transistor level flow (see Figure 3), the cell level flow does not require physical verification, initially.

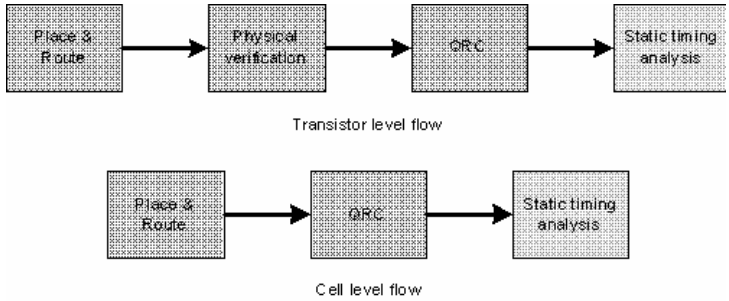

Figure 3 Transistor and cell level flow

The QRC parasitic extraction flow, which has been adapted for digital netlists, is depicted on Figure 4.

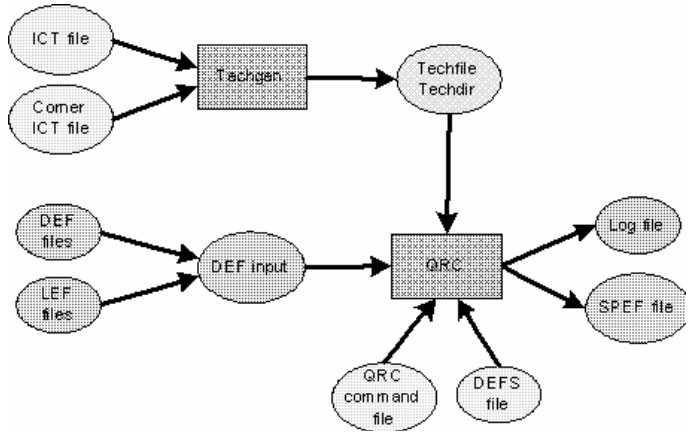

Figure 4 QRC parasitic extraction flow [4]

An important part of the extraction flow is the Techgen simulation. During parasitic extraction the Techgen data, which is contained in the technology file, is matched to the layout. When a match is found, the capacitance coefficients associated with the matched model are used to derive and extract the parasitic capacitance of the corresponding layout shape. Metal layer sheet resistance values in the technology file are used to calculate parasitic resistance values. If the QRC field solver is used, an internal mesh accurately models layout geometries and directly calculates parasitic capacitance [5].

Input files are:

- Design files (DEF) – files which contain a detail description of the design which will

be extracted. DEF are the outcome of the place and route phase

- Library files (LEF) – files that consist a detail definition of the content of each standard cell and mega cell, which is required. The library data can be contained in one or more LEF files in support of the DEF design files.
- Process description files (ICT and techfile) – files which contain binary technology capacitance models and design rules used by QRC to extract the interconnect parasitics. For resistance extraction, the technology file contains resistance information on each interconnect layer and via; for capacitance extraction, it contains three-dimensional interconnect models. QRC uses a technology file, created from the fabrication process information, along with the actual design data for resistance and capacitance extraction. The fabrication process information is entered into an ASCII-format process description file from which Techgen generates a technology file for QRC (see Figure 4). The compiled technology file contains a suite of three-dimensional adaptive analytical models that are generated for each process description.
- Commands file (CMD) – the QRC extraction process is controlled through the use of a command file, provided as input at the time of the execution. This is an ASCII file which is written in native QRC common command language and which QRC uses to define the various commands and options that the extraction run requires [4].
- Definitions file (DEFS) – this file contains an association of technology names with a path to the technology directory, one per line.

Output files are:

- Standard parasitic extended format file (SPEF) – compressed netlist file, which contains interconnect parasitic elements, which can be converted to delays for timing analysis tools. SPEF can be used with any delay calculator to produce a standard delay format (SDF) file used for simulation. The output file could also be in detailed standard parasitic format (DSPF). There is not any significant difference between them with the exception that SPEF netlist is in a compressed format, which reduces output file size by several times. In the proposed methodology, both files have been generated [4].
- Log file – file which contains detail information about the parasitic extraction, which has been carried out.

METHODOLOGY OF USE

First of all, the binary techfile needs to be created from a process description one per technology and corner. Each corner specifies a certain process variation and effect, such as minimum/maximum metal spacing, tallest/shortest wires, maximum/minimum surface area and so forth. The whole Techgen simulation usually consumes couple of hours.

The process is made up of several distinct steps (see Figure 5) which have to be performed for running techgen, as follows:

- Prepare a model plan – beginning with an ICT process description file, the first step is to devise plan files which are used to start many parallel jobs to create the interconnect models;
- Run techgen – making the interconnect models by launching the main model creation job on the LSF;
- Complete any incomplete jobs – If the models are not complete, then the missing models have to be manually made to resume creating the technology file;
- Combine the results in a technology file – the technology file is created by concatenating all models into a single file [5].

The commands, in details, for each of the steps above are:

```
Techgen -cell -plan -lsf_number 100 technology.ict
Techgen -cell -parallel -autoconcat technology.ict technology.tch
Techgen -cell incomplete incomplete.out
```

```
Techgen –cell –concat technology.ict technology.tch
```

QRC extraction is invoked on the shell command line with the following command:

```
qrc –cmd TSMC.cmd design.def
```

where: commands `qrc` and `cmd` invoke the parasitic extraction module and the command file, respectively;

`design.def` invokes the def input file.

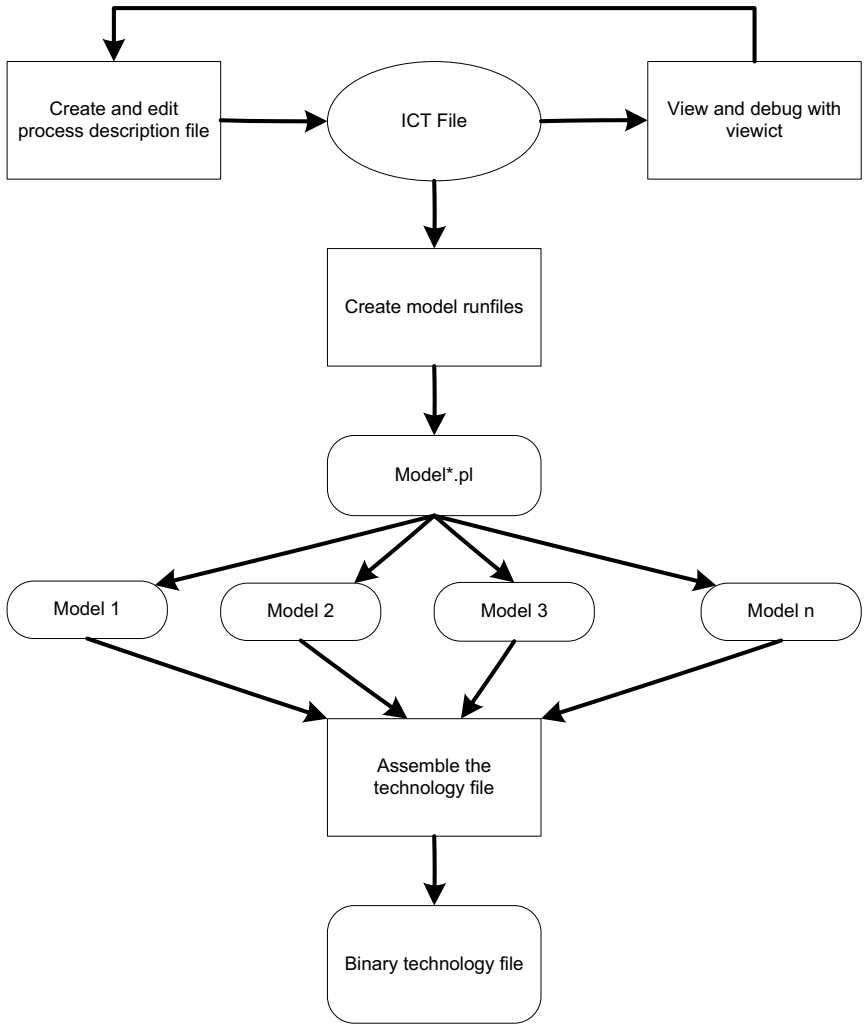

Figure 5 Techgen cell flow [5]

RESULTS

An extract of the generated SPEF file is shown bellow (see Figure **6**):

```
*10392_inst_testTop/inst_funcTop/u_top/u_sys/FE_OFC863_n2
*10393_inst_testTop/inst_funcTop/u_top/u_sys/FE_OFC862_n2
*233764_inst_testTop/inst_funcTop/u_top/u_sys/FE_OFN862_n2
*D_NET *233764 2.33418
*CONN
*I *10393:Y O *C 242.2 443.24 *D INVX2M
*I *10392:A I *C 244.44 436.52 *D CLKINVX4M
*CAP
0 *10393:Y 0.0830858
1 *10392:A 0.571258
2 *233764:2 0.49298
3 *233764:3 1.01192
4 *233764:5 0.174942
*RES
0 *10393:Y *233764:5 0.189913
1 *10392:A *233764:4 6.868
2 *233764:2 *233764:4 6.868
3 *233764:2 *233764:3 3.356
4 *233764:3 *233764:5 4.448
*END
```

Figure 6 An extract of the SPEF file

This extract corresponds to the schematic below (see Figure 7):

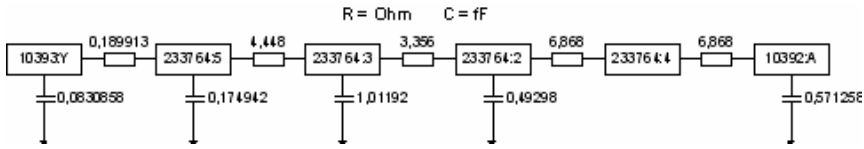

Figure 7 SPEF extract converted to a schematic

The pins 10393:Y and 10392:A and the net 233764 correspond in the overall design to the pins FE_OFC863_n2, FE_OFC862_n2 and the net FE_OFN862_n2, respectively. This is illustrated on Figure 8, where all metals have been removed with the exception of metal 1.

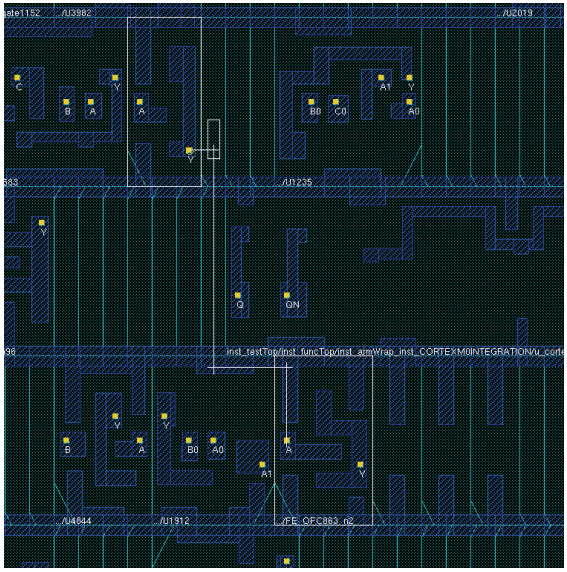

Figure 8 Extract of top layout

CONCLUSION AND FUTURE WORK

The paper has presented a comprehensive workflow and methodology for use of parasitic extraction. It provides an overview of the whole process of extraction of parasitic components, as well as gaining knowledge of any single stage amidst workflows, input and output data, commands and reviewing results.

Although, the paper is especially useful for anyone who has either not or limited previous experience, it could be of particular interest to everyone who is involved on the field of IC design, because additionally describes the state of the art and theoretical aspects of the Cadence QRC tool.

Looking at the near future, the parasitic extraction is going to assume greater and greater importance. At 130nm and below, signal delay due to interconnect parasitics becomes much more significant than the contribution to signal delay due to the inherent cell delays. Approximately 80% of the delay for most paths is due to interconnect delays [3,4].

However, it is also true that the accuracy of the parasitic extraction comes at a cost - in terms of run time to perform the extraction. It is a function of design size, process, desired results and the number and configurations of systems that are available to do the extraction.

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REFERENCES

[1] Martin G., Electronic Design Automation for Integrated Circuits, 2007

[2] Wang L., Cheng-Wen Wu, XiaoQing Wen, VLSI Test Principles and Architectures, 2009

[3] Xiaoning Q., R. Dutton, "Interconnect parasitic extraction of resistance, capacitance and inductance," 2003
[4] QRC Extraction Users Manual, Cadence, 2010
[5] QRC Techgen Reference Manual, Cadence, 2010

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Докладът е рецензиран.