THU-ONLINE-SSS-EEEA-02

ANALYSIS AND LAYOUT DESIGN OF CURRENT MIRRORS IN INTEGRATED CIRCUITS

Denis Sami, Bachelor Student
Department of Electronics,
Univesity of Ruse "Angel Kanchev"
Tel.: +359 89 990 3304
E-mail: denis.sami1997@gmail.com

Assoc. prof. Krasimira Stefanova Shtereva, PhD
Department of Electronics, Ruse,
Univesity of Ruse "Angel Kanchev"
Phone: +359 82 888 366, +359 88 993 5368
E-mail: KShtereva@ecs.uni-ruse.bg

Abstract: *An optimization of different current mirror topologies was made via simulation analysis and utilization of modern layout design methods. The investigated low voltage, short channel circuits operate with a supply voltage of 1.5 V. The current mirrors were simulated and design using 0.11 μm technology in a Virtuoso Cadence CAD tool. This investigation shows that high-performance circuits can be obtained by use of the cascode technique and other design solutions that reduce ratio errors due to nonideal effects.*

Keywords: *Current mirror, layout, Virtuoso Cadence.*

INTRODUCTION

In the last decades, Microelectronics has become the driving motor of the progress in many areas, such as information technologies, industrial electronics, medical electronics and car industry. An important role for those achievements has played the development in microelectronic technologies, and the new design circuit solutions used in integrated circuits design.

Current mirrors (CM) are the basic building blocks in the design of the integrated circuits (ICs). They are used as a current source or as an active amplifier load (Shtereva K., 2016, Kaur, J., 2017). Current mirror biasing is an important technique utilized in both, analog and digital circuits design.

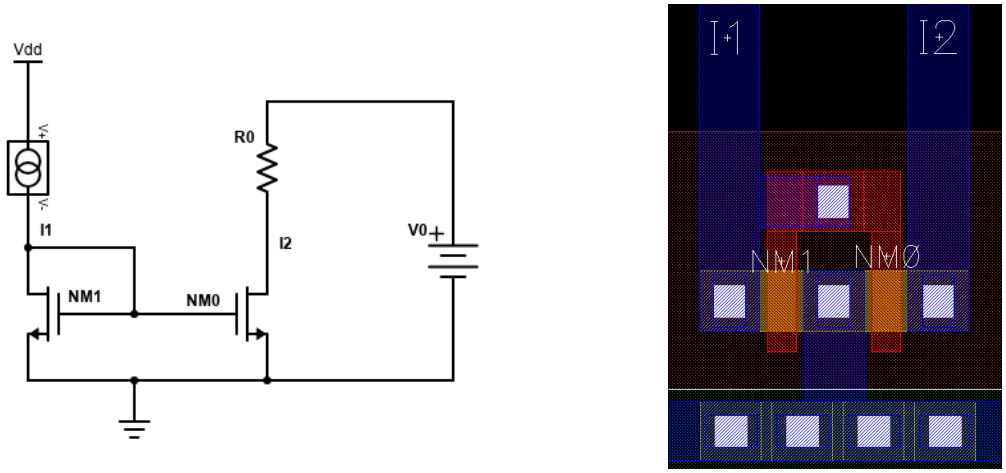
At present, the research efforts have been focused on development of the design techniques for low-voltage ICs in standard CMOS process. In (Rakus, M., 2018) was investigated the design approach involving the bulk-driven (BD) MOS transistors and dynamic-threshold (DT) MOS transistors. Three different CM topologies were analyzed. The authors found that both techniques can decrease by 30% the minimum output voltage of the improved Wilson and the cascade CM compared to the conventional gate-driven topology. Other group (Zohoori, S., 2018) proposed a low-voltage (1 V), low-power (1.4 mW) transimpedance amplifier in 90 nm CMOS based on a current mirror, for application in 10 GBps optical communications.

In this paper are presented five different current mirror topologies and their layout designs made in 0.11 μm CMOS technology, using a Virtuoso Cadence Computer-Added Design (CAD) tool. The simulation results for the dependence of the load current on the supply voltage were compared.

RESULTS

Basic current mirror

The simplest type of a current mirror consists of two matched *n*-channel MOS transistors. In Fig. 1(a) is shown a schematic and in Fig. 1(b) is shown a layout of the basic current miror.



(a) (b)

Fig. 1 Basic Current Mirror: (a) schematic; (b) layout.

The input current I_1 is defined by a current source. The output current I_2, "copies" or "mirrors" I_1. NM1 is a diode connected MOS transistor and works in saturation because $V_{DS1} = V_{GS1}$. In general, the ratio I_2/I_1 is given by the equation (Allen, Ph. E., & Holberg, D. R., 2002):

$$\frac{I_2}{I_1} = \left(\frac{\frac{L_1}{W_1}}{\frac{L_2}{W_2}}\right)\left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right)^2 \left[\frac{\lambda V_{DS2}}{1 + \lambda V_{DS1}}\left(\frac{k_2}{k_1}\right)\right] \quad (1)$$

L_1, L_2 – channel lengths of NM1 and NM0, W_1, W_2 – channel widths of NM1 and NM0, V_{T1}, V_{T2} - z threshould voltages of NM1 and NM0, k_1, k_2 – transconductance parameters of NM1 and NM0, λ - channel length modulation.

Hence, both MOS transistors are processed on the same integrated circuit $V_{T1} = V_{T2}$, $k_1 = k_2$. If $V_{DS1} = V_{DS2}$ the equation (1) can be rewriten:

$$\frac{I_2}{I_1} = \left(\frac{\frac{L_1}{W_1}}{\frac{L_2}{W_2}}\right) \quad (2)$$

The equation (2) gives the ideal ratio I_2/I_1 between the load and reference currents. This ratio is proportional to the width-to-length ratious, or aspect ratious, which are design parameters. The two transistors must be identical in order to obtain current ratio of 1:1. The non-accurate copying of the current in the basic current mirror is due to nonideal effects such as: channel length modulation; threshould voltage offset, and not perfect matching between the two transistors.

Output resistance of the basic current mirror is given by the formula:

$$r_o \cong \frac{1}{\lambda I_D} \quad (3)$$

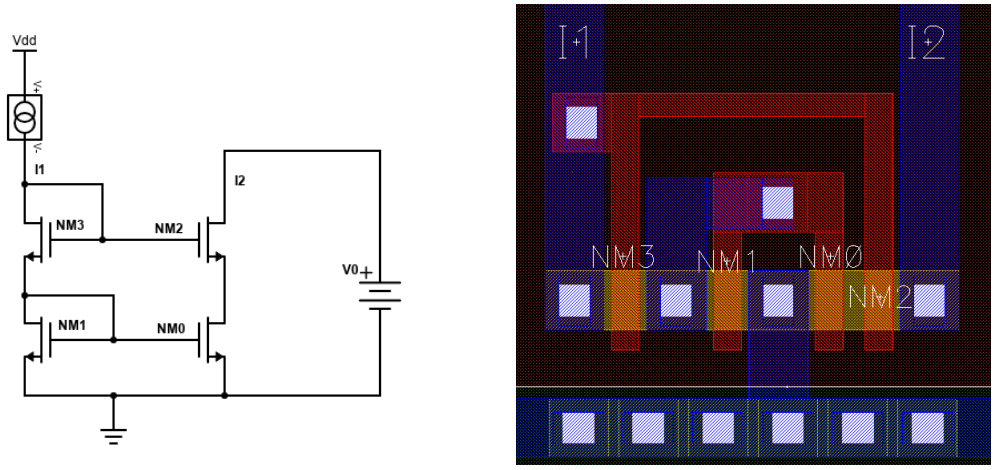
The output resistance is an important measure of the perfection of the circuit. It is relatively low for the basic CM.

The simplicity and the small chip area are the main advantages of this current mirror. The proposed layout (Fig. 1(b)) is designed so that to minimize the area.

Cascode current mirror

The utilization of the cascode technique reduses ratio errors due to: (i) differences in input and output voltages; (ii) neglecting of channel length modulation; (iii) and increasing the output resistance. Consecuently, the error in copying currents is reduced.

In Fig. 2 are shown: (a) the schematic, and (b) the layout of cascode current mirror.



(a) (b)

Fig.2 Cascode current mirror: (a) schematic; (b) layout

The cascode can consist of 3, 4, 5 or 6 transistors, depending on the desired precision in the current copying. The problem with many connected transistors is the increased power supply voltage level, which is in contradiction with the current microelectronic trends that require both, the reduction of the supply voltage and the size of the chip. The output resistance of the cascode current mirror is given as (Razavi, B. (2001):

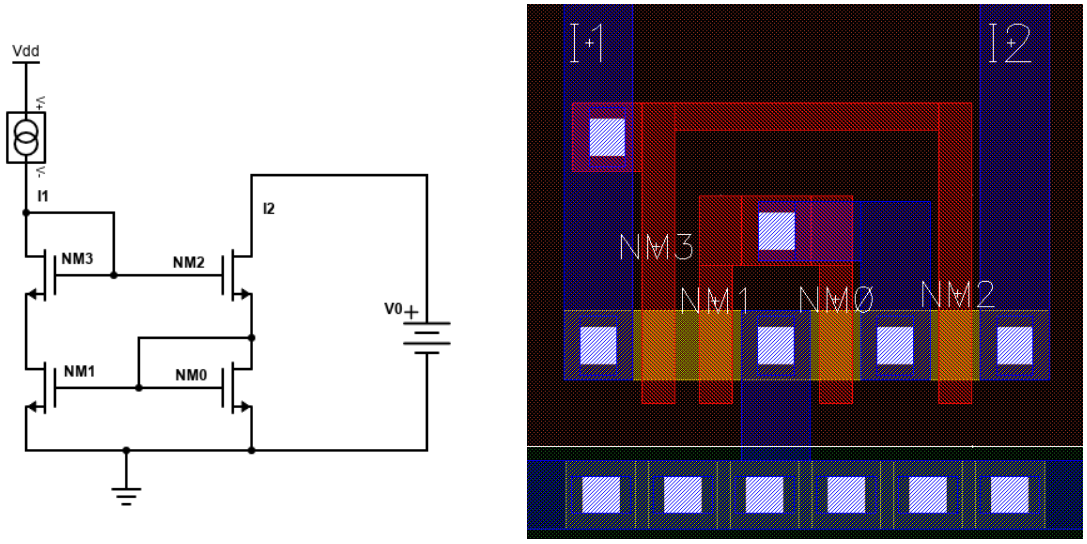
$$r_o = g_{m2} * r_{o2} * r_{o0} \quad (4)$$

The output resistance of the cascode current mirror is much higher than that of the basic one, hence, the load current is much stable against the variations of the output voltage (Reshma, P.G., 2017). The layout design (Fig. 2 (b)) ensures the reduction of parasitic elements and mismatch effects on the mirror's ratio.

In order to decrease the error in copying current, the four transistors must be in saturation mode. The diode connected NM1 and NM3 are in saturation. The transistors NM0 and NM2 will be in saturation if output voltage of NM2 drain is at least two times Vdsat (V_{dsat0} and V_{dsat2}). Hence, a minimum required supply voltage is about 1 V.

Modified Wilson cascode current mirror

This schematic (Fig. 3(a) is an improved version of the basic Wilson current mirror. **(**Spencer, R. 2001**).** As a result of the insertion of the NM3 transistor, the gate-source voltages of NM1 and NM0 are equal. The use of negative feedback improves the output resistance, which means beter current copying. The systematic error of the circuit is negligible. The physical design shown in Fig. 3(b). closely resembles the standard cascode CM. The only difference is that the NM1 and NM0 transistors have different connectivity, such that, the diode connected NM0 transistor is on the right branch.



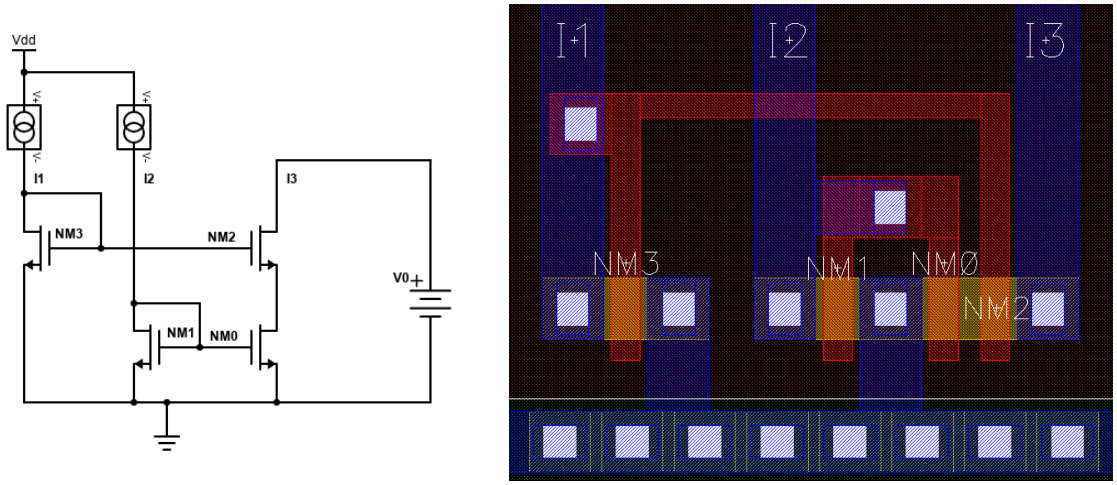
(a) (b)

Fig. 3 Full Wilson current mirror: (a) schematic; (b) layout

The obtained current characteristics (Fig. 6) show that the ratio error can be reduced if all four transistors operate in saturation. In this case the current copying is as good as for the standard cascade circuit. Because of that, nowadays, this architecture is rarely used in CMOS technology.

Wide swing cascode current mirror

The wide swing cascode current mirror shown in (Fig. 4 (a)) is a variety of the standard cascode current mirror for lower bias voltages (Arif, M., 2012). This wide swing cascode CM architecture needs additional current mirror branch to keep NM2 in saturation so that V_{dsat2} is much lower than normal cascoded current mirror. With this improvement the output voltage swing is higher than usual cascoded current mirror.



(a) (b)

Fig. 4 Wide swing cascode current mirror: (a) schematic; (b) layout

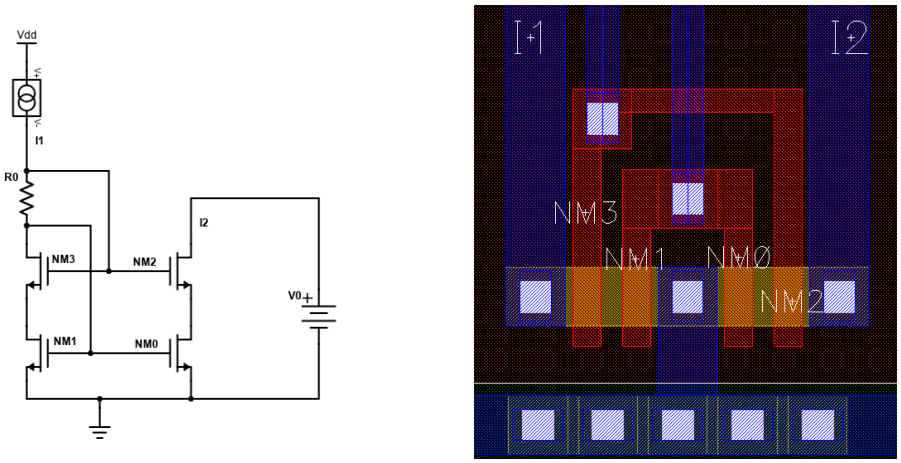
Of course, this scheme improves output swing, but it also brings with it a disadvantage associated with consumption as well as a need of second stable current. The basic functionality of the circuit is the following, the transistors except NM3 are the same. This single transistor is about 4 times larger channel than the other L in order to increase the drop required for NM2 to be saturated. The other option is that the current in branch one is 4 times larger, which is not good for the consumption of the current mirror. Since the cascode is biased from another referent current,

the operating point of cascode is chosen so that Vdsat is at a minimum, allowing higher output swing and lower power supply.

Layout (Fig. 4 (b)) takes up more space and the transistor finger matching are not quite well done, because of transistor NM3. These adjustments can be improved by applying dummy or spare transistors that aim to improve the mismatch of individual transistors.

Self-biased cascode current mirror

The advantage of this architecture (Fig. 5 (a)) is that it does not need a reference input current like the others (Guha, K., 2017). The reference current is generated by the resistor R_1. This resistor is required in order to obtain the correct V_{GS1} voltage to bring all four transistors to saturation. The value of the resistor is selected in order to provide a drop that drives the current mirrors into saturation.



(a) (b)

Fig. 5 Self-biased cascode current mirror: (a) schematic; (b) layout

The value of the resistor is about 50 kΩ, which requires a large chip area. The other problem is to realize a high resistivity resistor with low tolerance. The resistor size could be more than 10 times larger that of the current mirror. Of course, in a large scheme, these resistors can be arranged in such a way that the block becomes as compact and compact as possible, but this does not exclude the large space available. In Fig. 5(b) is shown the layout of a self-biased cascode current mirror.

Fig. 6 shows a comparative graph of the different topologies of current mirrors. The red color is a constant current I_1 = 10μA. The simulation results (Fig. 6) show that the current copying is the best for the self-biased cascode current mirror, and a reference current is not needed. Of course, the temperature-dependent and high-tolerance resistor can slightly degrade the current. This scheme is one of the most used in industry and plays an important role in a number of complex designs.

Other important parameters of the current mirrors, such as voltage swing, power consumption, power supply voltage and size of the layout, depend on the current mirror topology as well. The increase of the number of cascoded transistor rises the power supply, reduces voltage swing and the chip area increases. Basic current mirror or wide swing current mirror should be used when the high voltage swing is required. Hence, the selection of the topology depends on system or product requirements so that the trade-off between parameters and the chip area to be reached.

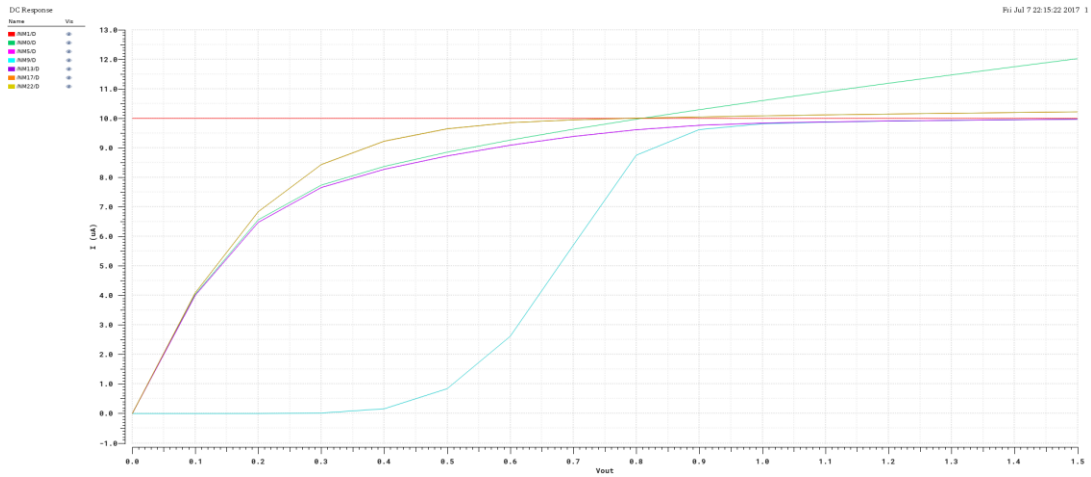


Fig. 6 Comparison of current mirrors topologies: Green line is for a basic CM; Purple line is for a cascode CM and a wide swing CM; Blue line is for a Wilson CM; Yellow line is for a self-biased and modified wide swing CM

CONCLUSION

In this paper are compared five current mirror architectures. The simulations and layout designs were made in 0.11 μm CMOS technology, using a Virtuoso Cadence. The simulation results show that the increase of the output resistance resulted in the improvement of the current copying, which becomes more stable over a number of variations. Another important parameter for a current mirror is the output voltage swing. The trade-off between accuracy, power consumption, and output voltage swing should be made in term of selecting "best" topology.

REFERENCES

Shtereva K. (2016). *Microelectronics*. University of Rousse "A. Kanchev". Ruse: Academic Printing house at University of Rousse "A. Kanchev", (***Оригинално заглавие:*** *Щерева, К. (2016). Микроелектроника. Русе: Русенски университет "А. Кънчев".)*

Kaur, J. (2017). Layout and Analysis of different Current Mirror using 45 nm Technology. *International Journal on Recent and Innovation Trends in Computing and Communication*, 5 (1), 239-243.

Rakus, M., (2018). Analysis of BD MOS and DT MOS Current Mirrors in 130 nm CMOS Technology. *Institute of Electronics and Photonics, Faculty of Electrical Engineering and Information Technology, Slovak University of Technology, Ilkovicova 3, 812 19 Bratislava, Slovak Republic*, 226-231.

Zohoori, S., (2018) A CMOS, low-power current-mirror-based transimpedance amplifier for 10 Gbps optical communications, *Microelectronics Journal*, 80 18-27.

Allen, Ph. E., & Holberg, D. R. (2002) *CMOS Analog Circuit Design*, 2nd Ed. , New York: Oxford University Press.

Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill.

Reshma, P.G., (2017). Analog CMOS implementation of FFT using cascode current mirror. *Microelectronics Journal* 60 30–37.

Spencer, R. (2001). Analysis of the Modified MOS Wilson Current Mirror: A Pedagogical Exercise in Signal Flow Graphs, Mason's Gain Rule, and Driving-Point Impedance Techniques. *IEEE TRANSACTIONS ON EDUCATION*, VOL. 44, NO. 4 322-328.

Arif, M., (2012). A Low Loss Wide Swing Cascode Current Mirror in 0.18-μm CMOS Technology. *Journal of Applied Sciences Research*, 8 (8): 4096-4102.

Guha, K. (2017). A Low Noise, High Gain OTA for Low Frequency Application. *4th International Conference on 'Microelectronics, Circuits and Systems'*.

