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ADVANCES IN THE DESIGN OF MINIATURE SINGLE-USE MEDICAL ENDOSCOPY CMOS IMAGE SENSORS[7]

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Abstract: *In this paper, a design procedure for an endoscopy sensor is proposed. The main topics are focused on the following parameters such as noise, speed, power, and area efficiency realized in the standard CMOS process. One of the major advantages of using CMOS technology is the opportunity that pixel and readout architecture are realized in the same wafer which leads to the design of compact sensors with advantages such as low pick-up noise from external sources, efficient row data processing from the photodetector, and high compatibility between internal modules. Thus leads to achieving a high yield from each die that reduces the final production cost. The reduction in cost makes the sensor suitable for a one-time usable device that relaxes the sterility requirements. The proposed system-on-chip finds application in bio-medical applications as in diagnostic medicine and especially for invasive surgery that leads to interventions with "minimal access".*

Keywords: *CIS, CMOS, Endoscope, Area and Consumption Efficiency, Bio-Medical Application*

INTRODUCTION

Recently the development of digital cameras in the field of medicine has seen significant advances in the last decade. The combination of the factors of miniaturization or the use of micro- or nano-technologies in medicine enables the design of measurement equipment leading to advantages in diagnostic medicine. An example of such a device is the endoscope (Zhang, M. 2008 & Erdogan, A, 2022), which serves for diagnostics, and the micro- and nano-technology is precisely the image sensor through which the inside of the body is reflected through natural openings. The advantages of the imagers as a bio-medical application help with "minimal access" surgery has become an increasingly preferred approach in multi-procedure and minimally invasive medical interventions, resulting in reductions in trauma, recovery time, complications, and final treatment costs. However, there are many challenges in minimal access surgery, which is based on the ability to localize the problem area through a micro-camera, for this purpose the demands on these devices are continuously increasing.

The structure is based on two technologies CCD and CMOS. The common components of the system are composed of an optical glass lens known as a micro-lens (optic part), a light source, and a sensor as an imager. One of the main differences between both technologies is the processing that could be done in- (CMOS) or -off (CCD) chip. The main disadvantages to realizing processing -off-chip, as it is done in a charged-coupled device (CCD), is viable the pick-up noise from external sources, reduced speed, and area requirements. That technology is known as the oldest compared to CMOS which has been used for more than a quarter of the last century. Due to a number of additional disadvantages from the consumer perspective of view such as lack of image quality, need for sterilization, and high production cost, the now-a-day trend in making endoscopes has shifted towards the use of CMOS technology that promises vital performance (Magnan, P., 2003). The CMOS image sensor (CIS) (Vatteroni M, 2010) is composed of a photodetector part composed of a pixel array followed by raw processing by analog and digital interface. The processed data is transferred via a communication channel that could be a flat ribbon, coaxial, or fiber-optic wires to

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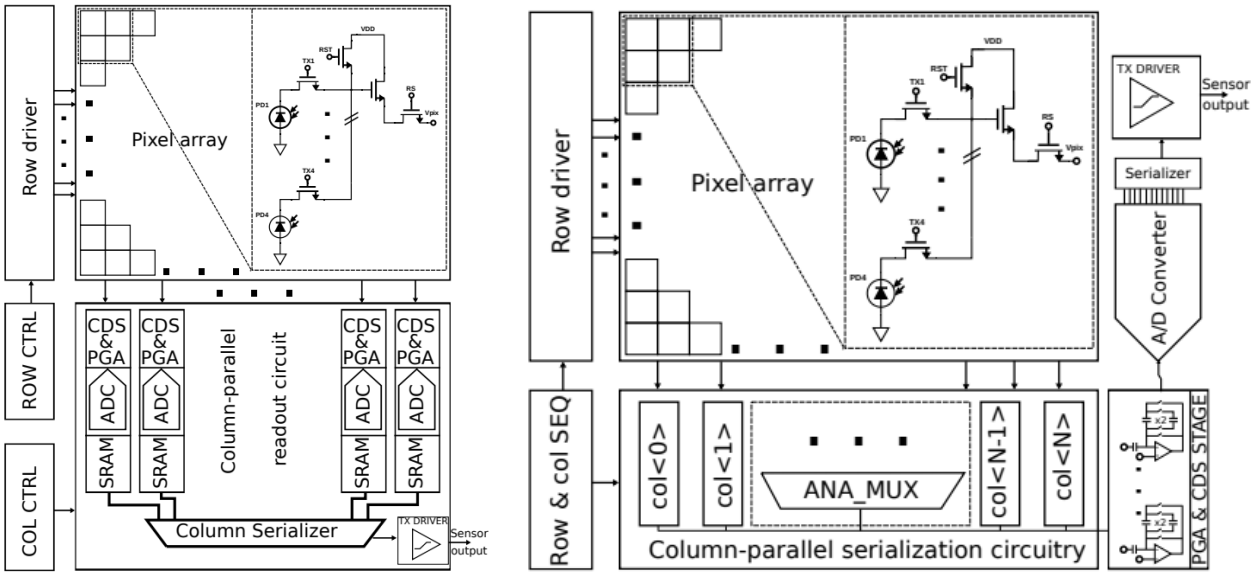
the receiver module which normally is an FPGA board (receiver). Although it is considered that CCD technology is fading, some of its great advantages such as low noise (high SNR) and high light sensitivity provide prerequisites for its preservation and development in other industries such as for space applications. The competition between CCD and CMOS continues to this day (Litwiller, D., 2001), but for medical purposes, CMOS technology is preferred because of its advantages and it is known as a video endoscope.

The CMOS technology is increasingly gaining popularity in the medical application market niche. The designed cameras achieve high integrity of photodetector and processing analog and digital interface logic in the same die that realizes system-on-chip. The obtained features are better resolution, speed, and energy efficiency, low pick-up noise from external sources as well as lower production costs with higher yields of semiconductor chips. The lower price and high yield make the devices single-time usable which removes the need for sterilization by toxic chemicals followed by the risk of long-time exposition of employees with a reduction in the sensor life cycle. Thus is one of the most vital features relative to CCD-based imagers (Mehta, S., 2015).

The aim of the proposed paper is to present architectural solutions and principles of the structure of a miniature endoscopic sensor based on the requirements of consumption, final physical size of the imager and system speed, as well as to structure concepts and constraints for the implementation of a physical layout, with the gradual upgrade from 2-D to 3-D technology.

CONVENTIONAL CIS ARCHITECTURE IN NOW-A-DAYS STATE OF THE ART

The architecture of CIS has been continuously developing for decades but the core design is not significantly changed. The principal structure is displayed in Fig. 1 a) from which can be concluded that the main parts that participate in processing data are pixel array, row driver, column-parallel processing, column serializer, and output (TX) driver. Auxiliary modules can include reference modules, internal memory, sequencer, oscillator, and phase or delay-locked loop circuitry that depends on the design specification and application.



a) Conventional CIS b) Compact CIS

Fig.1 Architecture Differences between Conventional and Compact Design.

The beginning of the raw data generation starts at the pixel. This is the device that converts the physical quantity "electromagnetic wave" into a charge domain by recombination of electrons. The pixels are realized by N columns and M rows create a so-called pixel array. Nowadays developments, active pixels are preferred with a structure that consists of a photodiode, several transistors, and an amplifier realized as a source follower. The pixel supports rolling or global

shutter mode of operation which depends mainly on structure and application. The aforementioned single-stage pixel amplifier helps with the transition from charge into the voltage domain on the one hand, as well as high-speed raw data transfer is accomplished through common vertical pixel buses on the other hand.

The control of the pixel array is carried out by means of signals generated by the rows. The sequence of generated control signals realizes the type of electrically controlled scanning known as a shutter with modes of rolling or global, as well as generation, storage, and control of the charge in the pixel.

The output data from the pixel is raw data that flows into columns in a parallel fashion. The read operation performed in all columns for the corresponding row is done globally since this type of data processing is called column-parallel processing. The column architecture differs from manufacturer to manufacturer depending on the necessary data processing and application of the sensor. The conventional CIS implementation includes modules such as a current source, a correlated double-sampling (CDS) circuitry, an amplification stage, and an ADC. Columns are read sequentially up to the last one, then start from the beginning for the next row. Last but not least classification depends on the communication channel between the sensor and receiver which could be in a serial or parallel fashion.

The requirements for speed, power consumption, and size of the sensor, three types of architectures implemented in CIS are known in state-of-the-art up-today. These architectures are primarily based on how the ADC supports the pixel array that is given as follows:

- Pixel level ADC mentioned in (Peizerat, A., 2007) and (Gamal, A., 1999) - the architecture offers the highest possible readout speed, but the consumption and occupied area are too high. It is not possible to realize a high-resolution array in order to meet moderate power consumption and optimal area requirements.
- Column-parallel level ADC - the architecture is one of the most preferred because it allows to achieve a relatively high speed while maintaining a moderate level of power consumption. The achieved optimal trade-off with column-parallel ADC supports individual columns or groups of pixel columns. The disadvantage is that the occupied area depends mainly on architecture. The advantage is that speed design consideration is relaxed, but it is difficult to achieve smaller size sensors as the single channel ADC-based sensors. A paper (Kawahito, S., 2018) discusses and compares the performance of CISs using column-parallel ADCs based on figures-of-merit and compares different A/D architectures.
- A single-channel ADC that supports the entire pixel array is the ideal choice for a miniature CIS image implementation, with a drawback of readout speed. The energy efficiency of this type of ADC directly depends on the architecture and desired speed, because the price to pay depends mostly on the desired sensor readout speed, designing a high-conversion speed architecture that is both compact and low-power is not a trivial task.

The advantage that single channel ADC architecture provides is the most suitable form to implement it into an endoscopy sensor.

DESIGN NOTES FOR ENDOSCOPY CIS IMPLEMENTATION

The difference in the design of the endoscopic sensor with respect to conventional CIS is observed and it is shown in Fig. 1b. One of the main parameters is the resolution of the array and the size of the individual pixel. Since the largest area is covered by the pixel array, the reduction is crucial in order to achieve compactness. Another important parameter to achieve compactness is the readout logic, preserving speed and power consumption, that the sensor can sink and dissipate since the sensor's dissipation power for a given final dimension is several times smaller than that of a standard imager.

The aforementioned challenges should be overcome in order to design a compact, fast, and energy-efficient CIS that can be applied as an endoscopy sensor.

Pixel Design Considerations

When designing the pixel, several parameters are taken into account, the most important for endoscopes being size and sensitivity, which are usually trade-offs. In Fig. 2 two-pixel architectures with time diagrams are shown, classified according to how a frame is captured (Le, T., 2015):

- Global shutter is one of the preferred image-capturing modes, as artifacts from fast-moving objects are removed. This type of pixel embedded in test vehicle sensors has been published in previous works in (Sami, D., 2021) and (Sami, D., 2022). The principle of operation is based on a memory located in the pixel, which makes it possible to store a full frame while readout the entire array. The drawback is the size that implements the additional memory, for this purpose, it is not applicable in miniature sensors.
- Rolling shutter is a simplified form of line-by-line image capture and does not require internal memory, which is the cause of artifacts (Baker, S., 2010), but allows for smaller pixel sizes.

Another important parameter is the trade-off between the size of the PD and gain, which on the one hand increases the signal-to-noise ratio, and on the other hand achieves greater light sensitivity or high-dynamic range (HDR), achieved by the small capacity of the photodiode.

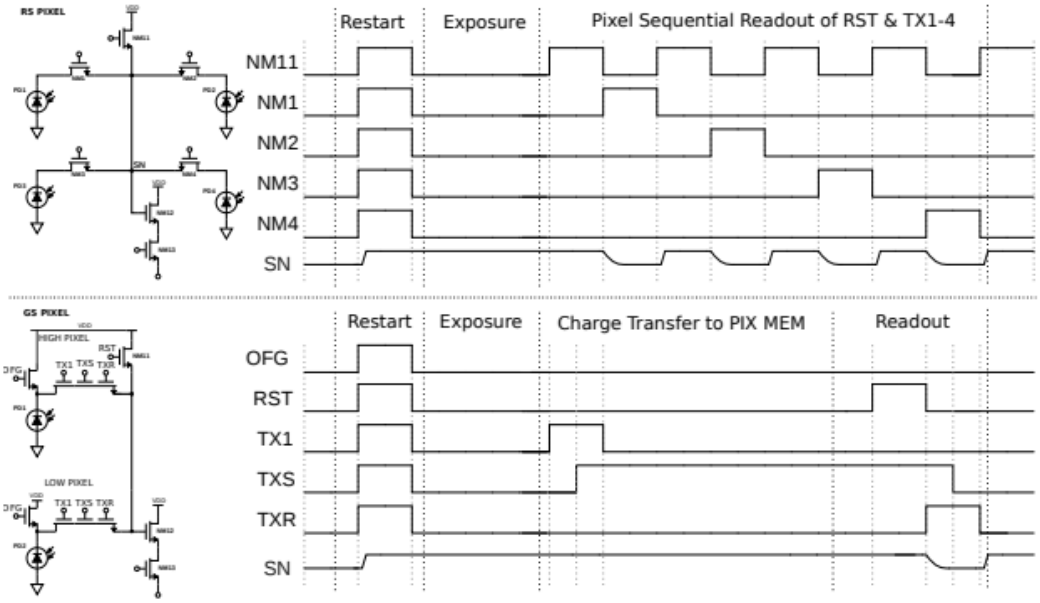
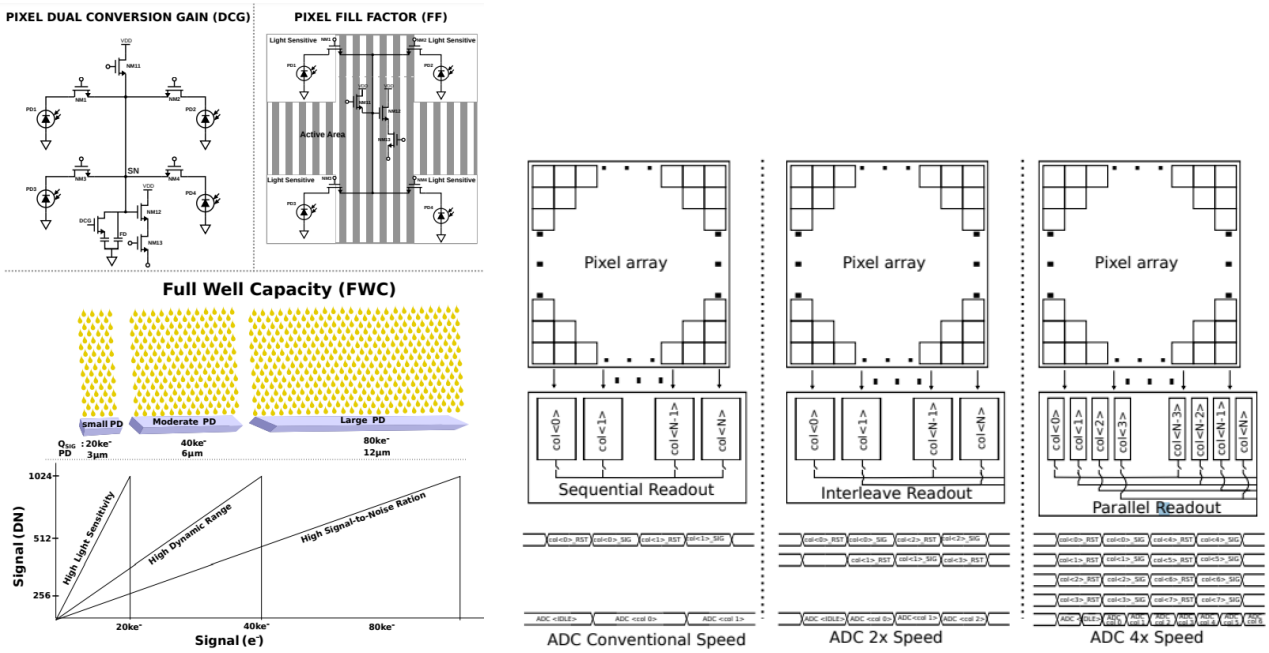


Fig. 2 Pixel Architectures and Timing: Global [GS] & Rolling [RS] shutter

The earliest gain is best done early in the circuit, and that is precisely in the pixel, being done in the charging region by means of a ratio of capacitors of photodiode CPD and floating diffusion CFD or sensed node CSN. The gain can be programmable if the additional capacitor is added in a parallel way to the FD or SN with a transistor in a switched mode known as dual conversion gain (DCG). As from Fig. 3a it has been shown that the gain can be statically set or programmable where the price to be paid is the increase in size.

Another important parameter is the fill factor ratio between the photodiode and the active part. This parameter aims to increase the area of the photo-detector part at the expense of the processing or readout part. The larger the photodiode is, the larger the Full Well and hence the light sensitivity based on more collection of charge based on light per exposure time. Another important part of the design of cube chip CIS is readout architecture.



a) Pixel DCG & FF & PD size Diagram b) Column Readout Architecture

Fig. 3 Pixel and Readout Architecture

Readout Design Considerations

In order to achieve compactness in the processing logic in the columns, it is mentioned to use a single channel ADC, but in order to serialize the data and sense it sequentially to the converter, a column-parallel logic is needed. The column voltage from the pixel output is sensed serially by single or several programmable amplifiers normally including a feature of correlated double sampling (CDS), followed by ADC. That column-parallel logic can be done in the following ways if speed is matter in addition to compactness shown in Fig.3 b). The timing diagram under each architecture shows the processing by column-parallel reading by emphasizing ADC conversion speed time. The highlighted versions have been used in various endoscope implementations that are within the scope of the thesis and are as follows:

- Sequential column-parallel architecture - the most conventional implementation when reading and processing the parallel raw data from the pixel. This type of architecture has been applied only to the smallest endoscope due to the advantages of the smallest area occupied and the simplicity of structure.
- Pipelined type of column-parallel architecture - the presence of a pipeline type of processing can be done when interleave techniques are used as data transfer and processing makes it possible to increase the processing time without affecting the speed (fps). This type of architecture is implemented in a large number of sensors.
- Parallel type column-parallel architecture - the presence of parallel data reading and processing makes it possible to increase the final speed of the sensor (frames/sec). This type of architecture is implemented in the fastest digital endoscopes.

Depending on the type of column-parallel architecture and the number of column buses, the number of programmable amplifiers with the CDS stage can also be different similar to the A/D Converter stages. Hence the connection of several programmable amplifiers to a single-channel ADC requires a ping-pong-based S/H circuit and logic that sequentially supports amplified and processed voltage to the A/D converter.

System Design Considerations

From a system perspective, the design requires some additional modifications in order to build an endoscopic sensor. These modifications are determined by the miniature size requirements which are as follows:

- The physical implementation of an endoscope follows schematic implementation and verification. The layout adheres to manufacturer-set rules to ensure practical feasibility. These rules, dictating the routing of individual elements, include limitations on bounding pad size for the sensor-receiver connection, considering reliability and manufacturability. Manual bonding constraints lead to a minimized number of pitches—four pads, comprising two for power supplies and two for half-duplex communication. These limitations necessitate prerequisites for autonomous control, achieved through internal signal generators and reference voltages. In-chip memory adds flexibility, allowing swift transitions from transmitter (TX) to receiver (RX) mode. Communication, depending on architecture and speed, occurs synchronously or asynchronously with the receiver.
- Speed determines whether the sensor operates synchronously or asynchronously. In synchronous communication, one wire handles clock frequency, and another handles output data. This approach is limited by pad load and speed, influenced by parasitics (RLC of the line). Although synchronous logic has speed limitations, it facilitates easier communication channel links with the receiver. Furthermore, asynchronous communication eliminates speed disadvantages by generating frequency within the sensor, freeing it from communication channel parasitics. However, achieving high speed in asynchronous mode increases complexity, demanding a stable internal oscillator for building robust communication links. Typically, various encoding techniques are applied to enhance robustness, but these details are beyond the scope of this work. In order to improve the robustness of the communication, various encoding techniques are usually applied that are not in the scope of this work.

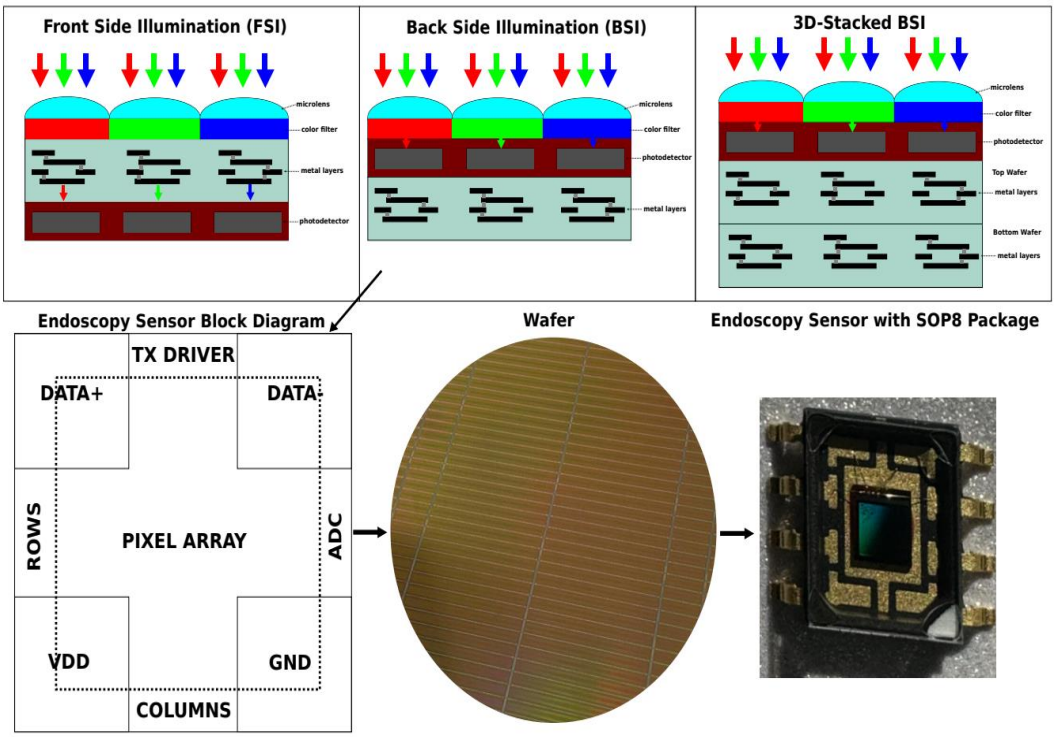


Fig. 4 System Revolution and Development Cycle

In the development of the microelectronic industry in the field of CIS, several technological revolutions are available that improve the functionality of the endoscopic sensor by relaxing the compactness requirements of both the pixel and the processing part displayed in Fig. 4, and they can be classified according to the layers and the direction of illumination:

- The oldest technology is called front-side illumination (FSI), the structure of which coincides with the conventional implementation of CIS. At the lowest level are the transistors, and above them the metals. It is important to note that routing is not recommended above the light-sensitive part (photo-detector), since a large part of the sensor

is made up of the pixel array, which complicates the connections between the individual modules in the system.

- The next important technology is back-side illumination (BSI), whose structure corrects the disadvantage of the previous one with routing because the illumination is done from the back of the sensor, which is in the shade and is free for inter-module connections. Another advantage is the deep photo-diode and short optical path, leading to a higher Quantum Efficiency (QE) and Lower Cross-talk.

The previous two technologies use a 2D-plane structure of the sensor and it is being compared in the following work (Taverni, G.,2018). The last revolutionary technology is the use of 3D stacking, which is similar to the layers in the implementation of a multi-layer printed circuit board (PCB). The technology distributes the system modules on several layers, that is, the pixels on the top layer, the columns and rows on another, and the internal memory on a separate one. This technology makes it possible to increase the resolution of a given sensor without changing the final sensor size and relaxes the area and routing requirements of the processing logic. Further improvement in 3D stacking technology was proposed by SONY (Fontaine. R., 2015) that PD and active pixel part including the amplification stage are also separated into layers that help to increase even more the resolution or increase pixel size to achieve higher sensitivity. The disadvantage of 3D stacking technology is the final production cost, as it is several times higher than the previous two technologies.

COMPARISON OF MINIATURE CIS REALIZED IN STANDARD CMOS PROCESS

From the advent of the first digital camera up to today, the CIS industry has seen significant progress in both academia and industry. Table 1 shows a classification of CIS achieved through scientific research, whose parameters such as pixel dimensions, resolution, speed, and final sensor size are specified to emphasize the design of compact sensors without speed degradation.

Table 1. Comparison of CIS proposed from Science

Sensor	Venezia, V., 2018	Mudassir, S., 2018	Wolfs, B., 2009	Larnaudie, F., 2017	Abbas, T., 2019	Ricardo M. 2017
Array Size	8MP	40K	160K	562.5K	16.4K	62.5K
Pixel Size	1.5µm	15µm	2.8µm	2µm	8µm	3µm
Speed	30fps	N/A	N/A	100fps	15fps	15fps
Sensor Size	N/A	3x3mm	1.78x1.78mm	N/A	1.4x1.4mm	1x1mm

In addition to the development and research communities, there are several CIS manufacturers who are developing CIS. In the indicated Table 2 the most compact sensors produced by some leading manufacturers in the CIS world are indicated.

Table2. Comparison of CIS proposed from Manufacturers

Company Name	**Sensor ID**	**Array Size**	**Pixel Size**	**Speed**
AMS	NanEye	62.25K	3µm	62fps
Omnivision	OV6948	40K	1.75µm	30fps
Always On	HM01BO	102.4K	3.6µm	60fps
Teledyne	Jade	550.4K	5.8µm	50fps
ONSEMI	ARX3A0	300K	2.2µm	360fps
Gpixel	GLUX160SBSI	480K	16µm	30fps

With the development of the microelectronics industry in the CIS, new market niches are constantly opening up in various branches of the digital imaging world, from where new companies are entering the industry. A new start-up company entering the world of line-scan sensors, which has Bulgarian roots called Photolitics, whose office is located in the city of Ruse. This creates prerequisites for the development of the microelectronics industry in the field of Digital Image Sensing followed by the realization of qualified designers, whose training was realized at University of Ruse „Angel Kanchev".

CONCLUSION

In the present development, architectural solutions and principles of the structure of a miniature endoscopic sensor are indicated. The strict requirements are consumption, final dimensions (sensor size), and speed of the system. The main parts to which these requirements are applied are the pixel array and the readout part. In addition to the structural level, basic physical layout implementation concepts and limitations are also shown, from where the paper is sum up with the technology development and gradual upgrade from 2-D to 3-D stacking technology with their advantages and disadvantages.

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