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# CHARACTERIZATION SYSTEMS FOR ENDOSCOPY SENSORS WITH ANALOG AND DIGITAL INTERFACES [2]

**Denis Sami, PhD Student**
Department of Electronics,
University of Ruse „Angel Kanchev”
E-mail: dsami@uni-ruse.bg

**Plamen Dikulakov, MSc**
Department of Electronics,
University of Ruse „Angel Kanchev”

**Prof. Aneliya Manukova-Marinova, DSc**
Department of Electronics, Ruse,
University of Ruse „Angel Kanchev”

**Deyan Levski, PhD**
Photolitics OOD, Ruse

***Abstract:*** *In this paper, we present a characterization system applied to the output communication interfaces of endoscopy sensors. It is focused on system output analog and digital interfaces as well as the impact of output data formats such as low-voltage signalling (LVDS = 200mV) and analog video (up-to swing 1.5V). Each system is extensively analysed from on-chip and off-chip perspective followed by the design of development boards for chip bring-up and system-optimizations through test-benches for real-time measurement and image processing. The paper analyzes the transfer between on-chip drivers though communication channel up-to receiver. The main topic is extended by suggesting decoding techniques of received raw data from the sensor in analog and digital domain in synchronous and asynchronous systems. The obtained results aim to asses the advantages and disadvantages of the proposed interfaces and depict the challenges in achieving robust communication channel.*

***Keywords:*** *CIS, CMOS, Endoscope, Bio-Medical Application, Analog and Digital Interfaces, LVDS, Communication Channel, Synchronous and Asynchronous System*

## INTRODUCTION

The development of endoscopic sensors has undergone significant milestones, transforming medical diagnostics and treatment methods. Endoscopy examinations began with Philip Bozzini's "Lichtleiter" in 1805, the first tool for examining internal cavities. In 1932, Rudolph Schindler introduced a flexible gastroscope, greatly improving accessibility and usability for internal imaging (D. Ramai., 2018).

The 1950s to 1980s saw a revolution with fiber-optic technology enabling real-time imaging. The introduction of video endoscopes based on CCD further enhanced image quality and diagnostic precision. Due to the benefit of low power consumption and easy system integration with on-chip circuits, recent advances in CMOS image sensors (CIS) have made them viable alternatives to charge-coupled (M. Bigas., 2006). The past decade has seen advances in the development of machine vision algorithms and methods for the visual training of neural networks. At this stage, there is an imbalance between the rate of development of the hardware required to supply machine vision systems with input data (captured images) and the subsequent image

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processing systems, usually implemented in the form of software programs.

In the 1990s, CMOS sensors revolutionized endoscopic technology (E. Fossum, 1997). These sensors offered energy efficiency, compactness, and scalability, leading to smaller, more portable devices. CMOS technology also improved resolution and frame rates, allowing for more accurate diagnostics. Their ability to integrate with digital processing supported advanced capabilities like 3D imaging, wireless systems, and capsule endoscopy, reshaping the possibilities of minimally invasive medical procedures. The CMOS technology can be applied in different forms as a endoscopy device that are described as follows:

1. Integration of CMOS Image Sensors in Endoscopy: CMOS sensors are being increasingly embedded at the distal tip of endoscopes, a design known as "chip-on-tip" (G. Matz., 2017) technology. This approach enhances image quality and reduces the bulk of the device, making it suitable for localized procedures such as biopsies. Advanced features like high frame rates (up to 60 fps) offer real-time imaging critical for precision surgeries. These systems also embedded the AntLinx™ interface (Photonics Spectra, 2021 Omnivision) for CMOS sensors, which optimizes data transmission over long cables, crucial for endoscopic applications. It minimizes pin count and system complexity while maintaining high image quality. This technology supports high-resolution imaging and cost-effective single-use endoscopes, improving patient safety and reducing cross-contamination risks.
2. Use in Disposable Endoscopes: Advances in CMOS manufacturing have made sensors affordable, enabling disposable endoscopes that mitigate the risks of cross-contamination associated with reusable devices (D. Covi, 2010). This innovation gained significant traction during the COVID-19 pandemic for procedures like bronchoscopies .
3. Beyond visible light sensing: CMOS sensors with near-infrared capabilities are expanding endoscopy applications, particularly for cancer diagnosis and treatment. NIR imaging enhances visualization of tissues and structures not visible in standard wavelengths, enabling targeted treatments like immunotherapies. (V. Venugopal, 2013).

These developments highlight the versatility and impact of CMOS sensors in advancing endoscopic imaging, improving both diagnostic precision and patient safety.

The conducted research involves the design of miniature CMOS light sensors with application in medical endoscopy. It aims to create new types of endoscopic sensors with a higher resolution and frame rate. Those imagers should support analog or digital interface contagion than the existing ones at this stage (Zhou, J., 2022). Additionally, the development of both a digital and analog test board that meets both communication standards for data transmission over a miniature interconnect wire is essential to verify the robustness of a communication link. The paper aims to qualitatively evaluate between digital (LVDS, LVTTL) and analog interfaces where the advantages and disadvantages are extensively discussed.

## COMMUNICATION LINK BETWEEN SYSTEM ON-CHIP AND IMAGE PROCESSING BOARD

The principle of a typical endoscope communication link between CMOS image sensor and receiver on board is depicted on Fig 1 which visualizes analog and digital communication interfaces. The cable that serves for interconnect (communication channel), must be selected according to its specification. The key parameters for endoscopy application are length (1 - 3m depends on medical application), wire cores as thin and low count as possible so that the minimum number is four: two for bi-directional communication, and two for power supply. ~~Proper~~ Individual shielding of the micro-coaxial for the analog interface in order to reduce EMI and self-coupling and external noise pick-up is essential for the reliable operation of the channel. Impedance-matched wire cores of the flat ribbon for the digital interface in order to satisfy bandwidth requirement that is reduced by physical limits introduced by RLC constants.

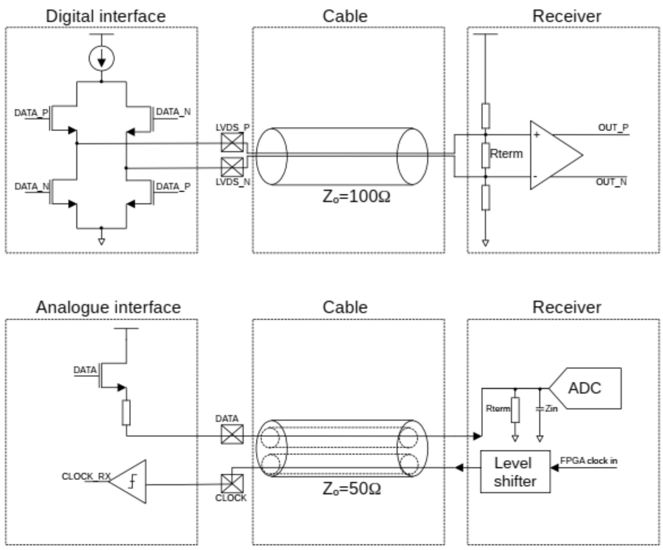
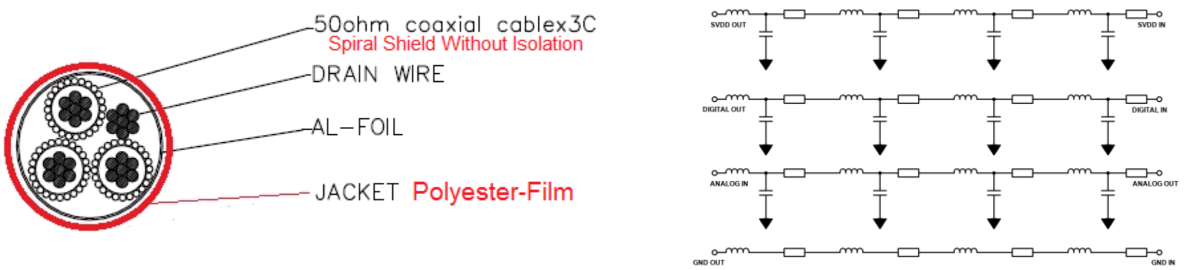



Fig. 1 Communication interface analog and digital between image sensor and on-board receiver

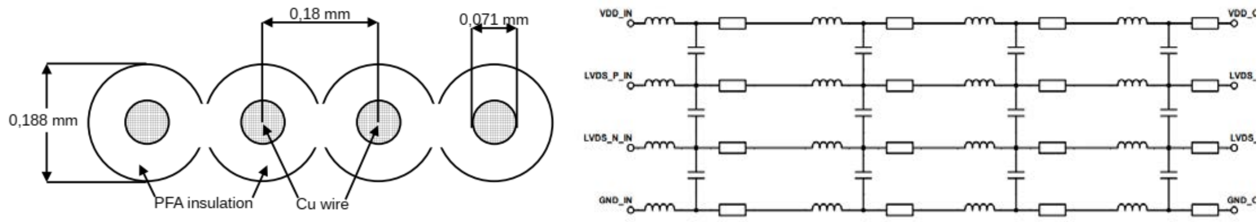
In the case of an analogue interface, the signal data path starts from on-chip source follower (SF), which represents a typical output driver of the system, goes through the micro coax cable shown in Fig. 2 with termination of far end (on-board) to digitize the video and convert it into digital 10-bit format by via an external on-board ADC. Each cable core is shielded in order to reduce coupling and interferences except ground as shown in Fig. 2 a). An equivalent distributed model is shown in Fig. 2 b) that is used to performed simulations and optimized trade-offs. The on-board termination also serves as a load of the on-chip SF that leads to additional flexibility in order to match different cable lengths in order to achieve proper signal headroom, bandwidth, gain, noise and consumption to satisfy the system requirements or meet specifications. The image sensor is synchronized by LVTTL clock going in reverse direction through second communication cable shielded pair. The voltage swing of clock path can be half or quarter of analog path in order to reduce noise coupling and interferences between two channels. Thus improves the quality of the signal transmitted through micro-coax cable.




a) Cross section b) Equivalent RLC distributed model

Fig. 2 Cross section and equivalent distributed model of the micro-coax cable used in analog interface

In comparison of digital interface, the signal path starts from the in-chip LVDS driver with programmable source termination resistor, goes through a flat-ribbon cable shown in Fig 3 terminated on far end. The shown cross section in Fig. 3 a) satisfy the distributed RLC model in Fig. 3 b) that is designed to optimized LVDS driver bandwidth, consumption and noise (as jitter) trade-offs. The termination is a part of receiver input so that the signal is decoded by high-speed comparator. The comparator induce amplification of the differential swing up-to 4 times so the eye opening is increased from 200mV to 800mV. The system embeds internal oscillator and operates in self-triggered mode in order relax pin requirements and satisfy 100 MHz bandwidth of communication channel realized by low-voltage differential signal. The synchronization between image sensor and receiver is achieved by clock data recovery technique that is trained through training pattern transmission between each row and frame.




a) Cross section b) Equivalent RLC distributed model

Fig. 3 Cross section and equivalent distributed model of the ribbon flat cable used in digital interface

**DEVELOPMENT OF TEST-PLATFORMS FOLLOWED BY OFF-CHIP PROCESSING**

The characterization and verification of the CIS with an analog output interface are performed using an evaluation board whose block diagram is shown in (Fig. 4a). The image sensor is connected to the test platform via a 1-meter micro-coaxial cable. The sensor's configuration is managed by the FPGA through an SPI interface. Once configured, the CIS begins streaming video, which is sampled by a 16-bit ADC.

The selected ADC offers several advantages: its high resolution (16-bit) enhances precision, its LVDS data output minimizes onboard switching noise, and its low sample-and-hold equivalent input capacitance (4 pF) reduces signal distortion. Inside the FPGA, the image processing pipeline starts by de-serializing and filtering the data to suppress noise. Subsequently, an image processing algorithm extracts meaningful pixel information from the full frame data.

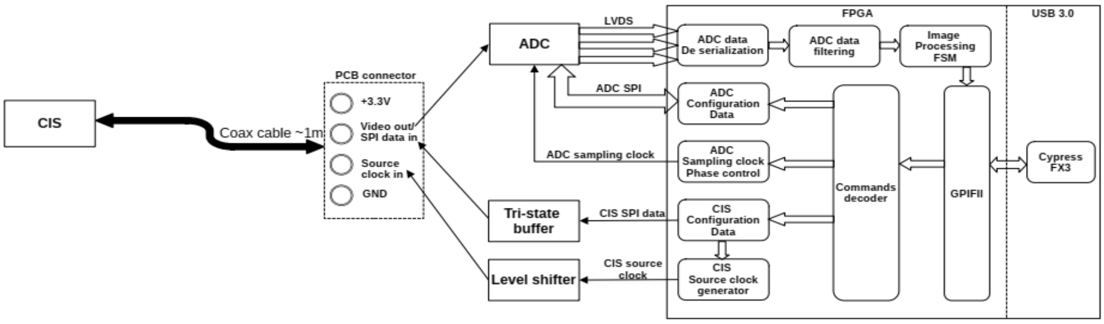
In the final stage, the GPIFII module formats the processed frame data and transmits it to a connected PC via the USB 3.0 interface. In the reverse direction, configuration commands, register values, and sampling clock phase and frequency settings are transmitted from the PC to the FPGA.

The block diagram in Fig. 4b illustrates the key components and principles of the development board used to evaluate a CIS with a digital output interface. As previously mentioned, the image sensor's output buffers can stream video in either LVTTL or LVDS mode.

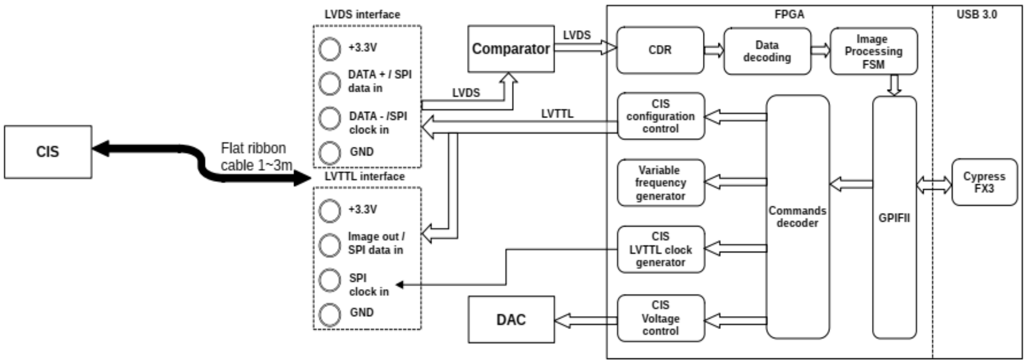
In LVTTL mode, the CIS is driven by an external clock generated by the "CIS LVTTL clock generator" implemented in the FPGA. The synchronous data stream is sampled at the falling edge of the source clock, which operates at a maximum frequency of 20MHz, resulting in a final video stream rate of 6fps.

In contrast, LVDS mode is designed for full CIS characterization and real-world medical applications, enabling a higher frame rate of 30 fps. In this mode, the image sensor output differential signal is processed by a comparator. The comparator compensates for the low current consumption of the CIS, which results in a differential swing that is lower than the minimum threshold required for the FPGA LVDS input receivers.

The streamed pixel data in LVDS mode is asynchronous, requiring processing by a Clock and Data Recovery (CDR) module. The CDR synchronizes the input frame data with the internal timing by oversampling the incoming data at four times the input bit rate. This module also includes a FIFO to ensure clock domain synchronization (Fig. 7b).




a) Analog interface characterization board;



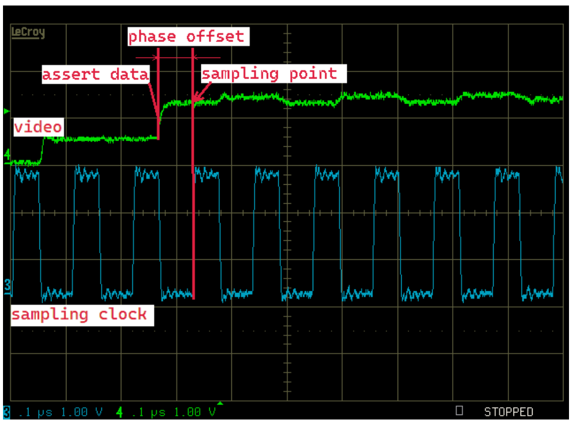

b) Digital interface characterization board

Fig. 4 Block diagram of development boards for endoscopy sensor with digital and analog interface

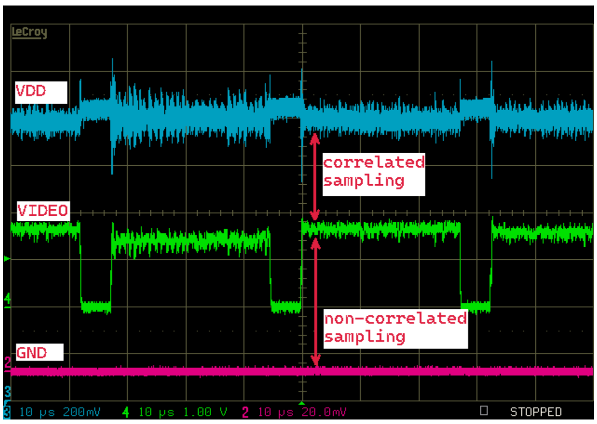
Similar to the analog interface characterization platform, the "Image Processing FSM" module arranges the pixel data into an array. The "GPIFII" module then formats the processed frame data and transmits it to a PC via the USB 3.0 interface.

## MEASUREMENTS, EVALUATION AND ASSESSMENT

One of the major challenges in sampling analogue video signal is to avoid the point where crosstalk occurs between the video data line and the source clock. Another significant issue is the overshoot at the start of each video line, caused by line driving. A process of selecting the optimal sampling point can be carried out as follows: first, the image sensor was placed in complete darkness. Then, the phase of the sampling clock was shifted relative to the supply clock in 20° steps (Fig. 5a). At each step, 100 images were captured, averaged, and a histogram was generated (Fig. 6). The optimal sampling point was determined as the point where the mean value of the temporal noise was at its lowest value.




a)Analog video signal with synchronous clock




b) in-chip SF interference in power supply

Fig. 5 Images taken from oscilloscope for an analog signal measurements

Figure 5b illustrates the influence of driving the video data line relative to the power supply. There could be few major techniques for video sampling, two of which are: non-correlated, and correlated sampling. Non-correlated sampling is a straightforward method that uses a single ADC input to sample the video signal. This method is usually used by oversampling the video data with sample rate 2x or 3x higher than the frequency of the sourced clock. Which means that for each pixel word, there are multiple data points (2 or 3), and their values could be averaged, effectively reducing noise and improving signal accuracy. This approach is simple but does not account for noise or variations caused by the power supply.

In contrast, correlated sampling is a more advanced method that utilizes two ADC inputs: one for the video signal and another for the power supply. During post-processing, the algorithm compensates for variations in pixel data caused by voltage drops due to in-chip drive kickbacks caused by the Source Follower (SF). This technique improves the accuracy of the reconstructed video signal by mitigating power-related noise.

The analogue interface research revealed that in case when video data is sampled by single ADC, the optimal sampling point should has 120º-140º phase offset relative to sensor clock.

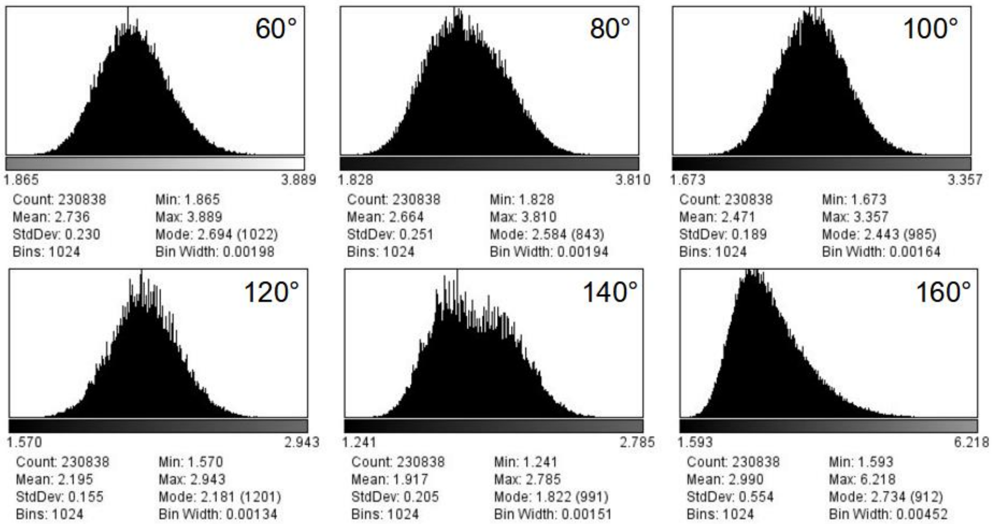
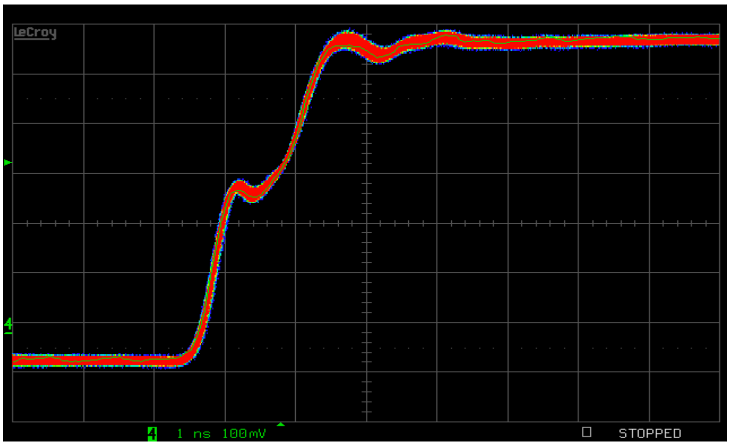
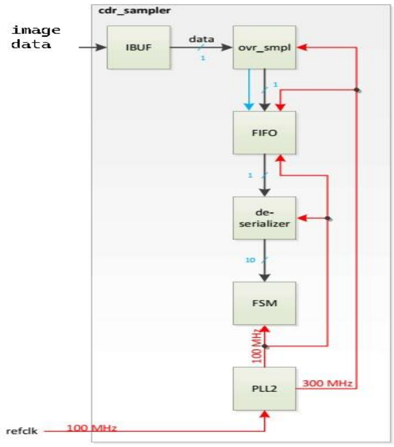



Fig 6: Histograms of the temporal noise captured in dark at different sampling clock phase offset

When the image sensor data is asynchronous, a critical component of the reconstruction pipeline is the Clock and Data Recovery (CDR) module (Fig. 7b). Its role is to synchronize the input data rate (100 MBps) with the FPGA internal timing. The module performance is constrained by jitter tolerances, allowing for a maximum of <5 ns jitter between consecutive words and <100 ns jitter between consecutive lines.




a)




b)

Figure 7: Digital interface measurements and techniques to recover data from LVDS protocol: a) Jitter in LVDS data line measured after 3m flat ribbon cable; b) Algorithm of CDR technique

During the development of the CDR algorithm, it was found that with 3x oversampling, there were edge cases where the CDR missed bits, leading to data reconstruction errors. To address this, 4x oversampling was implemented, which significantly improved the robustness of the module, making it more resilient to input data uncertainties.

## CONCLUSION

The presented evaluation and investigation of interface architectures highlight the different interfaces for miniature endoscopic sensor. Key performance requirements for such an imagers include low power consumption, compact sensor size, system speed, and robust communication with a board-level FPGA. The choice of output interface depends heavily on the specifications of the application and the robustness of off-chip signal transmission, which is followed by image processing on the system onboard configuration.

This work explores both analog and digital output interfaces. Analog communication channels are more resistant to high electromagnetic interference (EMI) sources, such as electrosurgical knives, making them a more robust choice in such environments. However, this robustness comes at the cost of reduced image quality. Conversely, when high image quality is a priority, digital data transmission should be used. The trade-off between robustness and image quality is highly application-specific and must be carefully evaluated based on the requirements of the medical use case.

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