FRI-2G.303-1-CCT1-04

# SUPPORTING DEVELOPMENT TOOLS FOR FPGA-BASED TRAINING PROCESSORS [4]

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***Abstract:*** *Experiments with programmable logic devices such as Field Programmable Gate Array (FPGA) have found their place in the lab exercises within various computer engineering courses, especially hardware-oriented ones. FPGA-based training processors, developed as course assignments have proved to be a useful educational tool for studying the basic concepts of computer architecture. One of the advantages of this approach is that students can experiment with different microarchitectures while they reconfigure their projects and modify the instruction set, addressing modes, and machine word size. In the Computer Systems and Technologies Bachelor Curriculum, the Design Technology (DT) course is a precursor to the Computer Architecture (CA) course, and in this sense, lab exercises with FPGA-based training processors will establish a fundamental knowledge base that will help the students better understand the more complex concepts taught in the CA course. This paper presents an overview of the major educational tools prepared for DT lab assignments: a family of educational processors, an assembler, and an assembly language simulator. One of the main requirements for the tools is to be customizable in terms of the machine type, instruction set, and machine word size of the target FPGA-based processor. Several examples are given to show how these hardware and software tools are used in the teaching process.*

***Keywords:*** *Computer Architecture, CPU, FPGA-based Processor, Instruction Set, Addressing Mode, Assembler, Simulator.*

This paper is awarded the "**Best Paper**" **Crystal Prize** and is published in the compiled proceedings *Reports Awarded with "Best Paper" Crystal Prize of the 63-rd Annual Scientific Conference of the University of Ruse and Union of Scientists – Ruse, ISBN 978-954-712-951-1 (Print); e-ISBN 978-954-712-952-8, pp. 41-47, https://conf.uni-ruse.bg/bg/docs/cp24/bp/bp-4.pdf*

**ACKNOWLEDGEMENT**

This work is published with the support of project 24-FEEA-01 "Methods and tools for automated analysis, processing, storage and management of multimedia data and documents", financed by the "Scientific Research" fund of Ruse University "Angel Kanchev".

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[4] The paper was presented on 25 October 2024 in section "Communication and Computer Technologies" with original title in English: SUPPORTING DEVELOPMENT TOOLS FOR FPGA-BASED TRAINING PROCESSORS

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